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## IN THE CLAIMS

1. (currently amended) An integrated circuit substrate comprising:  
a first surface for receiving a series of aligned layers during the creation of the integrated circuit, and  
a second surface disposed substantially opposite the first surface, the second surface having no layers formed thereon and at least one alignment mark formed thereon prior to the first surface receiving any of the series of aligned layers during the creation of the integrated circuit, the at least one alignment mark adapted for aligning the series of aligned layers one to another during the creation of the integrated circuit.
2. (original) The substrate of claim 1 wherein the second surface is divided into a first half and a second half, with one alignment mark in each of the first half and the second half.
3. (original) The substrate of claim 1 wherein the second surface is divided into quadrants, with one alignment mark in each of the quadrants.
4. (original) The substrate of claim 1 wherein the at least one alignment mark is printed on the second surface.
5. (original) The substrate of claim 1 wherein the at least one alignment mark is recessed into the second surface.
6. (original) The substrate of claim 1 wherein the at least one alignment mark comprises geometric shapes in a pattern.
7. (withdrawn)
8. (original) An integrated circuit, the improvement comprising a series of aligned layers aligned upon at least a portion of the substrate of claim 1.
9. (withdrawn)
10. (withdrawn)

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11. (withdrawn)
12. (withdrawn)
13. (withdrawn)
14. (withdrawn)
15. (withdrawn)
16. (withdrawn)
17. (withdrawn)
18. (withdrawn)
19. (withdrawn)
20. (withdrawn)